CLAIMS

24. A method of forming a line of FLASH memory cells comprising:

forming a line of floating gates over a semiconductor substrate;

providing an alternating series of trench isolation regions and active area regions in the semiconductor substrate in a line adjacent and along at least a portion of the line of floating gates, the series of active areas defining discrete transistor source areas separated by trench isolation regions, the trench isolation regions comprising isolation trenches having insulating dielectric material received therein;

forming a conductive line over the discrete transistor source areas and over the insulating dielectric material received within the isolation trenches adjacent and along at least a portion of the line of floating gates, the conductive line electrically interconnecting said discrete transistor source areas; and

providing source forming conductivity enhancing impurity into the discrete transistor source areas.

25. The method of claim 24 wherein a majority of the source forming impurity is provided before forming the conductive line.

26. The method of claim 24 wherein a majority of the source forming impurity is provided commensurate with or after forming the conductive line.

27. The method of claim 24 comprising providing the series of trench isolation regions before forming the line of floating gates.

28. The method of claim 24 wherein the conductive line comprises conductively doped polysilicon capped with a conductive silicide layer.

29. A method of forming a line of FLASH memory cells comprising:

forming a line of floating gates over a semiconductor substrate;

providing an alternating series of trench isolation regions and active area regions in the semiconductor substrate in a line adjacent and along at least a portion of the line of floating gates, the series of active areas defining discrete transistor source areas separated by trench isolation regions;

forming conductively doped semiconductor material over the discrete transistor source areas and trench isolation regions separating same adjacent and along at least a portion of the line of floating gates which electrically interconnects said discrete transistor source areas;

out diffusing source forming conductivity enhancing impurity into the discrete transistor source areas from the conductively doped semiconductor material; and

patterning the conductively doped semiconductor material into a conductive line.

30. The method of claim 29 wherein the conductively doped semiconductor material is capped with a conductive silicide layer.

31. The method of claim 29 wherein the conductively doped semiconductor material is capped with a conductive silicide layer prior to the patterning.

36. (Twice Amended) A method of forming a line of FLASH memory cells comprising:

forming a line of floating gates over a semiconductor substrate, the line of floating gates having a source side and a drain side, the line of floating gates having an insulative cap having an outermost surface;

depositing an insulative sidewall forming layer over the line of floating gates; and

in one anisotropic etching step of the insulative sidewall forming layer, forming an insulative sidewall spacer on only the drain side and not on the source side by masking the source side with masking material during the one anisotropic etching step, the insulative sidewall spacer having an outermost surface which is substantially elevationally coincident with the insulative cap outermost surface.

37. (Twice Amended) A method of forming a line of FLASH memory cells comprising:

forming a line of floating gates over a semiconductor substrate, the line of floating gates having a source side and a drain side, the line of floating gates having an insulative cap having an outermost surface;

depositing an insulative sidewall forming layer over the line of floating gates;

in one anisotropic etching step of the insulative sidewall forming layer, forming a first insulative sidewall spacer on only one of the source side and the drain side and not the other by masking the other with masking material during the one anisotropic etching step, the first insulative sidewall spacer having an outermost surface which is substantially elevationally coincident with the insulative cap outermost surface; and

further comprising in another anisotropic etching step, forming a second insulative sidewall spacer on the other side, the second insulative sidewall spacer having an outermost surface which is substantially elevationally coincident with the insulative cap outermost surface.

39. The method of claim 36 wherein no insulative sidewall spacer is ever formed on the other side.

40. The method of claim 37 wherein the one side is the source side.

41. The method of claim 37 wherein the one side is the drain side.

45. The method of claim 24 wherein the isolation trenches are filled with said insulating dielectric material.

46. The method of claim 24 wherein the conductive line has a substantially planar outermost surface.

47. The method of claim 24 wherein the conductive line has a substantially planar innermost surface.

48. The method of claim 24 wherein the conductive line has a substantially planar outermost surface and a substantially planar innermost surface.

49. The method of claim 31 wherein the trench isolation regions comprise isolation trenches having insulating dielectric material received therein and the conductive line is formed over the insulating dielectric material received within the isolation trenches.

50. The method of claim 49 wherein the isolation trenches are filled with said insulating dielectric material.

51. The method of claim 31 wherein the conductive line has a substantially planar outermost surface.

52. The method of claim 31 wherein the conductive line has a substantially planar innermost surface.

53. The method of claim 31 wherein the conductive line has a substantially planar outermost surface and a substantially planar innermost surface.

54. The method of claim 36 wherein the semiconductor substrate comprises monocrystalline silicon.

New Claims

Please add new claims 55-60 as follows:

55. (Added) The method of claim 24 wherein the line of floating gates is formed over channel active area of the semiconductor substrate and is formed to have a source side and a drain side, the forming of the line of floating gates comprising providing a gate dielectric layer intermediate floating gate material and the channel active area, the forming of the line of floating gates comprising initially etching through the gate dielectric layer on the source side and not on the drain side.

56. (Added) The method of claim 25 wherein the line of floating gates is formed over channel active area of the semiconductor substrate and is formed to have a source side and a drain side, the forming of the line of floating gates comprising providing a gate dielectric layer intermediate floating gate material and the channel active area, the forming of the line of floating gates comprising initially etching through the gate dielectric layer on the source side and not on the drain side.

57. (Added) The method of claim 26 wherein the line of floating gates is formed over channel active area of the semiconductor substrate and is formed to have a source side and a drain side, the forming of the line of floating gates comprising providing a gate dielectric layer intermediate floating gate material and the channel active area, the forming of the line of floating gates comprising initially etching through the gate dielectric layer on the source side and not on the drain side.

58. (Added) The method of claim 29 wherein the line of floating gates is formed over channel active area of the semiconductor substrate and is formed to have a source side and a drain side, the forming of the line of floating gates comprising providing a gate dielectric layer intermediate floating gate material and the channel active area, the forming of the line of floating gates comprising initially etching through the gate dielectric layer on the source side and not on the drain side.

59. (Added) The method of claim 36 wherein the line of floating gates is formed over channel active area of the semiconductor substrate, the forming of the line of floating gates comprising providing a gate dielectric layer intermediate floating gate material and the channel active area, the forming of the line of floating gates comprising initially etching through the gate dielectric layer on the source side and not on the drain side.

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60. (Added) The method of claim 37 wherein the line of floating gates is formed over channel active area of the semiconductor substrate, the forming of the line of floating gates comprising providing a gate dielectric layer intermediate floating gate material and the channel active area, the forming of the line of floating gates comprising initially etching through the gate dielectric layer on the source side and not on the drain side.